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10EC/TE71

Seventh Semester B.E. Degree Examination, June/July 2016
Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the ISO – OSI reference model with suitable diagram. Discuss the functions of each layer. **(10 Marks)**

b. Describe the SS7 signaling and services with suitable model. **(06 Marks)**

c. The internet users in the year January – 2015 is 50,000. It will roughly doubling in size for every 18 months. What is the expected number of internet users in the year December 2026? **(04 Marks)**

2 a. Generate CRC code and check if there is any error in the code word. If data word is 1001 and divisor is 1011. How these are implemented using encoder and decoder? **(10 Marks)**

b. Explain stop-and-wait ARQ protocol with suitable timing diagram. **(06 Marks)**

c. A channel has a bit rate of 4 Kbps and a propagation delay of 20 msec. For what range of frame sizes does stop and wait protocol give an efficiency of at least 50%? **(04 Marks)**

3 a. Discuss the behaviour of the three persistence methods of CSMA. **(06 Marks)**

b. Discuss three channelization protocols. **(09 Marks)**

c. A group of N stations share a 56 Kbps pure ALOHA channel. Each station outputs a 1000 bit frame on an average of once every 100 sec. What is the maximum value of N? **(05 Marks)**

4 a. Explain 802.3 Ethernet frame format and addressing technique. **(10 Marks)**

b. Briefly discuss the distributed co-ordination function and point co-ordination function of 802.11 MAC sub-layer. **(10 Marks)**

PART – B

5 a. Discuss the loop problem in bridged LAN. How loop problems are solved in bridged LAN? **(10 Marks)**

b. Differentiate between a bus back bone network and star back bone network. **(06 Marks)**

c. What characteristics are used to group station in a VLAN? **(04 Marks)**

6 a. Explain class full addressing. What are default masks? **(06 Marks)**

b. Find the class full address :

i) 125·05·13·8
ii) 225·06·13·8
iii) 14·23·120·5
iv) 220·06·120·5. **(04 Marks)**

c. An ISP is granted a block of addresses starting with 190·100·0·0/16. The ISP needs to distribute these addresses to three groups of customers as follows :

i) The first group has 64 customers ; each needs 256 addresses
ii) The second group has 128 customers ; each needs 128 address
iii) The third group has 128 customers ; each needs 64 addresses

Design the sub blocks and find out how many addresses are still available after these allocations. **(10 Marks)**

7 a. Explain the distance vector routing for following graph. **(10 Marks)**

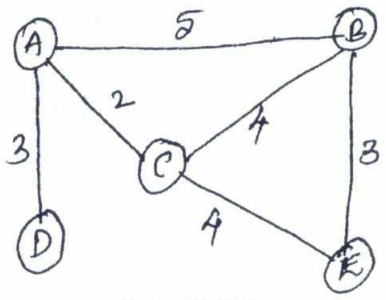

Fig. Q7(a)

b. Find a shortest path three for following graph using Dijkstra algorithm. **(10 Marks)**

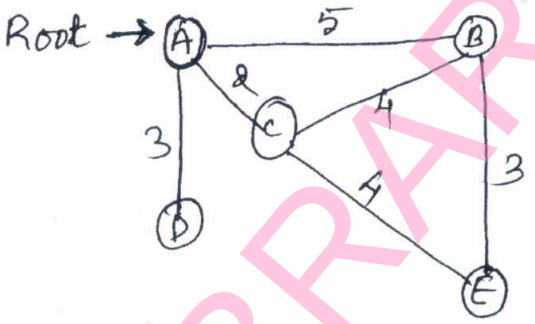

Fig. Q7(b)

8 a. Explain three way hand shake based connection establishment in TCP. **(10 Marks)**

b. Explain the different field in UDP, with suitable diagram. **(06 Marks)**

c. Differentiate between connection less and connection-oriented service. **(04 Marks)**

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10EC/TE72

Seventh Semester B.E. Degree Examination, June/July 2016
Optical Fiber Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Discuss the advantages of optical fiber communication. **(06 Marks)**

b. With the help of neat diagrams discuss the structure of single mode and multi mode step index fibers with appropriate mathematical equations. **(06 Marks)**

c. Estimate the maximum core diameter for an optical fiber with refractive index difference of 1.6% and a core refractive index of 1.48, in order that it may be suitable for single mode operation for an operating wavelength of 0.9 μm. Further estimate the maximum core diameter for a single mode operation when the relative refractive index difference is reduced by a factor of 10. Assume V number as 2.405. **(08 Marks)**

2 a. Discuss different types of non linear scattering losses. **(06 Marks)**

b. Silica has an estimated fictive temperature of 1400 K with an isothermal compressibility of 7×10^{-11} m^2N^{-1}. The refractive index and photoelastic co-efficient for silica are 1.46 and 0.286 respectively. Determine the theoretical attenuation in decibels per kilometer due to fundamental Rayleigh scattering in silica at optical wavelength of 0.63 μm. Boltzmann's constant is 1.381×10^{-23} JK^{-1}. **(08 Marks)**

c. A step index multimode fiber with a core refractive index of 1.500, a relative refractive index difference of 3% and an operating wavelength of 0.82 μm. Estimate the critical radius of curvature at which large bending losses occurs. **(06 Marks)**

3 a. Explain with the help of neat diagram, distributed-feedback (DFB) laser diode. **(06 Marks)**

b. A double-hetrojunction In GaAsP LED emitting at a peak wavelength of 1310 nm has radiative recombination times of 30 and 100 ns, respectively. The drive current is 40 mA. Find the following:
i) The bulk recombination life time.
ii) The internal quantum efficiency.
iii) Internal power level (assume electron charge as 1.602×10^{-19} C) **(07 Marks)**

c. Discuss the operation of pin photodetector with appropriate diagrams. **(07 Marks)**

4 a. With appropriate mathematical equations explain single-mode fiber joints. **(06 Marks)**

b. Explain fusion splicing of optical fibers with appropriate diagrams. **(06 Marks)**

c. Briefly describe the principal of operation of the following:
i) Expanded beam connector.
ii) Star couplers. **(08 Marks)**

PART – B

5 a. With a schematic diagram, explain the working of an optical receiver. **(06 Marks)**

b. Explain the term receiver sensitivity. Derive an equation for receiver sensitivity in terms of photo detector noise. **(08 Marks)**

c. Discuss coherent detection with relevant block diagram. **(06 Marks)**

6 a. Discuss subcarrier multiplexing. **(06 Marks)**

b. Explain link power budget with a relevant diagram. **(06 Marks)**

c. Write a short note on:

i) Chirping.

ii) Extinction ratio penalty. **(08 Marks)**

7 a. Explain the principal of operation of WDM with relevant block diagram. **(07 Marks)**

b. Discuss the design and operation of a polarization independent isolator made of three miniature optical components. **(06 Marks)**

c. Explain with help of relevant diagrams various application of fiber Bragg gratings. **(07 Marks)**

8 a. With the help of energy level diagrams, explain the working of Erbium-Doped Fiber Amplifiers (EDFA). **(10 Marks)**

b. Write short notes on :

i) SONET / SDH frame formats.

ii) High-speed lightwave links. **(10 Marks)**

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10EC73

Seventh Semester B.E. Degree Examination, June/July 2016
Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the different types of power electronic converter circuits with neat circuit diagram and input and output waveforms. Also mention its application. **(08 Marks)**

b. Write the symbol and characteristic features of the following devices:
(i) BJT (ii) TRIAC (iii) GTO (iv) MOSFET. **(08 Marks)**

c. Discuss the peripheral effects of power electronic converters. Also write the remedies. **(04 Marks)**

2 a. For the circuit shown in Fig.Q2(a), the BJT is specified to have β in the range of 12 to 75. If V_{cc} = 40 V, R_c = 1.5 Ω, V_B = 6 V, $V_{CE(sat)}$ = 1.2 V and $V_{BE(sat)}$ = 1.6 V and R_b = 0.7 Ω. Calculate: (i) Overdrive factor ODF (ii) Forced B_f (iii) Total power dissipation(P_T) **(07 Marks)**

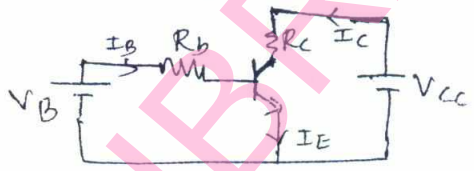

Fig.Q2(a)

b. With the transient model of MOSFET explain switching characteristics. **(06 Marks)**

c. What is the need for isolation for gate drive circuits? Discuss the different methods of providing isolation of gate drive circuits from power circuits. **(07 Marks)**

3 a. Explain the V-I characteristics of SCR by clearly indicating different states on characteristics. Also explain different modes of operation. **(06 Marks)**

b. With two transistor analogy of a thyristor obtain the equation for anode current. **(06 Marks)**

c. An SCR employs an R-triggering as shown in Fig.Q3(c) with $I_{g(min)}$ = 0.1 mA and $V_{g(min)}$ = 0.5 V. The diode is silicon and the peak amplitude of the input voltage is 24 volts. Determine the triggering angle α for R = 100 kΩ and R_{min} = 10 kΩ. **(04 Marks)**

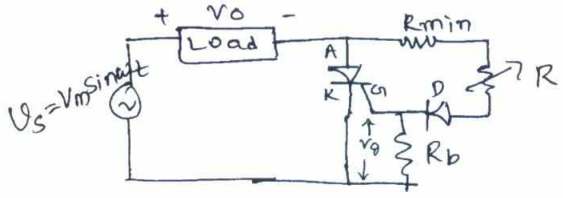

Fig.Q3(c)

d. A SCR has a di/dt = 50 A/μsec and dv/dt = 150 V/μsec. It operates on a 100 V, calculate the snubber circuit elements using approximate expressions. **(04 Marks)**

4 a. With necessary circuit and waveforms explain the principle of operation of single phase semiconverter. Also derive an expression for the average output voltage. **(06 Marks)**

b. With neat circuit diagram explain the operating principle of dual converter with and without circulating current. **(08 Marks)**

c. A single phase half wave controlled rectifier is used to supply power to 10 Ω load from 230V, 50 Hz supply at a firing angle of 30°. Calculate (i) average output voltage (ii) effective output voltage (iii) average load current. **(06 Marks)**

PART – B

5 a. What is the necessary condition for successful commutation of SCR? Compare between forced and natural commutation. **(06 Marks)**

b. With necessary circuit and waveforms explain the working of complementary commutation. Also perform circuit analysis. **(08 Marks)**

c. For the impulse commutated thyristor of circuit Fig.Q5(c), determine the turn-off time of the circuit, if V_s = 200 V, R = 10 Ω, C = 5 μF and $V_c(t = 0) = V_s$. Also derive the equations used. **(06 Marks)**

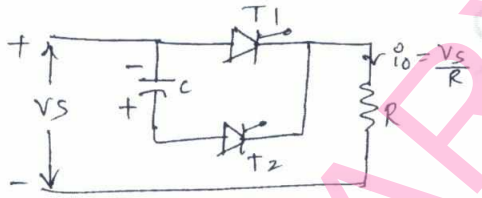

Fig.Q5(c)

6 a. With the help of neat circuit and relevant waveforms explain the working of ON-OFF control, for single phase AC voltage controller with resistive load. Also derive an expression for RMS output voltage. **(08 Marks)**

b. A 1 ϕ half wave ac voltage controller has an input voltage of 120 V, 60 Hz and a load resistance of 10 Ω. The firing angle of thyristor is 60°. Find
(i) RMS output voltage (ii) Input power factor (iii) Average input current. **(08 Marks)**

c. What is the problem caused by sharp single pulse triggering in a 1 ϕ AC voltage controller when the load is inductive? How can this be solved? **(04 Marks)**

7 a. Briefly explain the classification of choppers with circuit, waveforms and quadrant diagrams. **(08 Marks)**

b. For the chopper shown in below Fig.Q7(b), DC source voltage is 200 V, load resistance is 20 Ω. Consider the voltage drop of 4 V across chopper when it is ON. For a duty cycle of 0.6, calculate (i) Average and rms value of output voltage. **(04 Marks)**

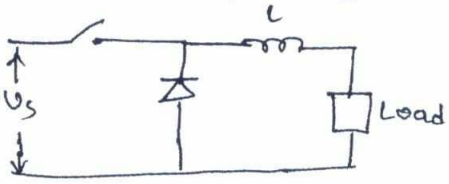

Fig.Q7(b)

c. Explain the operation of step down chopper with RL load. Also derive an expression of peak-peak output ripple current. **(08 Marks)**

8 a. Explain the principle of single phase half bridge inverter with suitable circuit and waveforms. **(10 Marks)**

b. Explain the performance parameters of inverter. **(04 Marks)**

c. Explain principle of working of variable DC link inverter. Also mention advantages and disadvantages. **(06 Marks)**

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10EC74

Seventh Semester B.E. Degree Examination, June/July 2016
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is an embedded system? List out three kinds of computing engines that are utilized in embedded system. **(04 Marks)**

b. Briefly describe the major elements of embedded system development life cycle. **(08 Marks)**

c. Define: i) Watch dog timer ii) Instruction cycle
iii) Hard real time system iv) Soft real time system **(08 Marks)**

2 a. Briefly describe the more commonly used addressing modes. **(08 Marks)**

b. Describe the four operations of instruction cycle in ISA and RTL level. **(06 Marks)**

c. Write short notes on finite state machines. **(06 Marks)**

3 a. Write short notes on:
i) Overlays
ii) Dynamic RAM with read and write operation timing. **(08 Marks)**

b. A system specification requires an SRAM system that can store upto 4K × 16 bit words, however the longest memory size available is 1K × 8 bit. Assume the processor having 16 address and data lines. Show the SRAM design for the above specification with read and write timing diagram. **(06 Marks)**

c. Explain in detail direct mapped cache design with word size of 32 bits for:
i) Cache size of 64K words organized as 128 0.5k word blocks.
ii) Main memory size of 128 M words organized as 2k pages holding 128 blocks each. **(06 Marks)**

4 a. What is a product life cycle and explain briefly V life cycle and spiral mode. **(08 Marks)**

b. List out the five steps and its importance in the design process of a successful embedded system design. **(06 Marks)**

c. Briefly describe the three areas that should be considered in static analysis of a system design. **(06 Marks)**

PART – B

5 a. Define thread. Enumerate the difference between a process and a thread. **(05 Marks)**

b. Write short notes on foreground/background system. **(05 Marks)**

c. What is a scheduling strategy? Define the three general categories of scheduling strategy. **(04 Marks)**

d. Explain the core responsibilities of operating system. **(06 Marks)**

6 a. Explain in detail about TCB (Task Control block) and its functions. **(06 Marks)**

b. Briefly explain about interrupts and its importance in developing kernel of embedded software. **(06 Marks)**

c. Describe the different kinds of stack that one might find in an embedded application. **(08 Marks)**

7 a. What is Amdahl's law? Consider a system with the following characteristics. The task to be analysed and improved currently executes in 100 time units and the goal is to reduce execution time to 80 time units. The algorithm under consideration in the task uses 40 time units. Calculate the amount of improvement required. **(05 Marks)**

b. Write short notes on Big 'O' notation. **(05 Marks)**

c. Perform the complexity analysis for loop constructs:

i) for loop

```
int sum = 0;
for (int j = 0; j < n; j++)
 sum = sum+j;
```

ii) while loop

```
int prod = 1;
int n;
while (! Done)
{ prod = prod*n;
 n – –;
 if(n < = 1)
done = true;
 }
```

(10 Marks)

8 a. Define response time. Describe the major components of response time analysis of (i) polled loop, (ii) pre-emptive schedule in an embedded application. **(08 Marks)**

b. What are the common mistakes that might be made during performance optimization analysis? **(05 Marks)**

c. How can we measure and reduce the effect that a software algorithm can have on power consumption? **(07 Marks)**

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10EC751

Seventh Semester B.E. Degree Examination, June/July 2016
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. An analog signal is sampled at the rate of 8 KHz, if 512 samples of the signal are used to compute DFT, X(k), determine the analog and digital frequency spacing between adjacent X(k) elements. Also determent analog and digital frequencies corresponding to k = 64. **(06 Marks)**

b. List the major architectural features used in DSP system to achieve high speed program execution. **(06 Marks)**

c. Explain the decimation and interpolation with equation. Let x(n) = [3, 2, –2, 0, 7]. It is interpolated using an interpolation filter b_k = [0.5, 1, 0.5] with interpolation factor–2. Determine the interpolation sequence. **(08 Marks)**

2 a. With a neat block diagram explain about the saturation logic and its use. **(06 Marks)**

b. Briefly explain about the 4 × 4 Braun multiplier with its structure. In n × n parallel multiplier structure how many adders are required? **(08 Marks)**

c. With a neat block diagram, explain address generation unit of DSP system. **(06 Marks)**

3 a. Compare architectural features of TMS320C25 and motarala fixed point DSP devices. **(06 Marks)**

b. Describe the multiplice/address unit of TMS320C54XX processor with a neat block diagram. **(06 Marks)**

c. Consider that AR3 is selected as the pointer for the circular buffer. The various register contents are B_k = 40, AR3 = 1020H, AR0 = 0025H. Find : i) start and end address of the buffer ii) contents of AR3 after the execution of the instruction LD *+AR3(12H)% iii) contents of AR3 after the instruction LD * AR3 + 0%. **(08 Marks)**

4 a. Explain the operation of serial input/outputs ports and hard ware timer of TMS320C54XX on chip peripherals. **(08 Marks)**

b. Differentiate between MAC and MACD instruction by way of explaining them. **(04 Marks)**

c. By means of a figure, show the pipeline operation of the following sequence of TMS320C54XX instruction. Assume initial value of AR3 is 80h and the values. stored in memory locations 80h, 81h, 82h as 1, 2 and 3

```
LD * AR3+ , A
ADD # 1000h, A
STL A, * AR3 +.
```

(08 Marks)

PART – B

5 a. What do you mean by Q–notations used in DSP algorithm implementation? What are the values represented by 16 bit numbers N = 4000h, in Q_{15}, Q_7 and Q_0 notations? **(08 Marks)**

b. Write an assembly language program for TMS32054XX processor to multiply two Q_{15} numbers to produce Q_{15} result. **(05 Marks)**

c. With the help of a block diagram, explain the implementation of an FIR filter in TMS320C54XX processor. Show the memory organization for the filter implementation. **(07 Marks)**

6 a. Why zero padding is done before computing the DFT? **(02 Marks)**

b. Explain an 8-point DIT-DFT implementation structure based on the butterfly on the TMS320C54XX. **(08 Marks)**

c. Determine optimum scaling factor to prevent over flow. **(10 Marks)**

7 a. Draw the I/o interface timing diagram for read–write–read sequence of operation. **(06 Marks)**

b. Design an interface to connect a 64k×16 flash memory to a TMS320C54XX device. The processor address bus is A_0 to A_{15}. **(06 Marks)**

c. What are interrupts? How interrupts are handled by the C54XX DSP processor? **(08 Marks)**

8 a. Explain with a neat diagram, the synchronous serial interface between the C54XX and a CODEC device, **(06 Marks)**

b. Explain the operation of pulse position modulation (PPM) to encode two biomedical signals. **(08 Marks)**

c. Describe with a suitable diagram a digital model for production of speech signal. **(06 Marks)**

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10EC/TE762

Seventh Semester B.E. Degree Examination, June/July 2016
Real Time Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the real time systems. Explain the computer control system of a hot air blower with a neat diagram. **(10 Marks)**

b. Define:
i) Clock based system,
ii) Event based system,
iii) Interactive based system. **(06 Marks)**

c. Write any four responsibilities of control engineer. **(04 Marks)**

2 a. What do you mean by adaptive control? With a neat diagram, explain any two types of adaptive control. **(10 Marks)**

b. Explain the following:
i) Supervisory control system,
ii) Distributive system. **(10 Marks)**

3 a. Explain parallel computers concepts with SISD, SIMD, MIMD and MISD with its advantages and disadvantages. **(10 Marks)**

b. Explain process related interface with suitable example. **(10 Marks)**

4 a. How do strong data typing contribute to the security of programming language? **(06 Marks)**

b. Explain the approaches of application oriented software. **(08 Marks)**

c. What is cutlass and what are the major requirements of CUTLASS? **(06 Marks)**

PART – B

5 a. With a neat block diagram, explain the typical structure of RTOS. **(10 Marks)**

b. What is meant by code sharing? Explain reusable and reentrant code. **(07 Marks)**

c. Define: i) Live lock, ii) Dead lock. **(03 Marks)**

6 a. Explain: i) Task chaining and swapping, ii) Task overlaying. **(07 Marks)**

b. Explain the task management system with states of tasks. **(07 Marks)**

c. Explain scheduling policies. **(06 Marks)**

7 a. Explain the different phases involved in the design of RTS. **(10 Marks)**

b. Explain foreground and background system with flow chart. **(10 Marks)**

8 a. Explain Yourdon methodology. **(05 Marks)**

b. Explain with relevant diagrams the Ward and Mellor method. **(07 Marks)**

c. Write about the environmental model, with context diagram for drying oven. **(08 Marks)**

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